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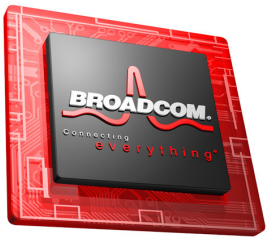
BCM8155
PRODUCT Brief



Multirate Low-Power 10G RZ/NRZ/Duo-binary Transceiver with 10G Clock

FEATURES

- Fully integrated multirate CDR, DEMUX, MUX, CMU
- 300-pin Multisource Agreement (MSA) compatible
- Compliant with ITU GR-253, XFP, and SFP+ specifications
- 16-bit LVDS interface compliant with Optical Internetworking Forum (OIF) SFI-4
- Programmable RZ/NRZ/Duo-binary modes
- Adjustable duty cycle in RZ mode
- RX equalization for ISI compensation
- Limiting amplifier
- RX phase adjustment
- Adaptable RX decision threshold adjustment
- 10G serial transmit clock output with adjustable phase
- 10G serial TX preemphasis
- PRBS generator/checker for built-in self-test (BIST)
- Line and system loopback modes
- Receiver and transmitter serial data polarity inversion
- LVDS polarity inversion and bit order reversal
- Analog loss-of-signal output (ALOSB) and loss-of-signal input (LOSIB)
- CMU and CDR lock detect
- FIFO overflow alarm
- Reference clock: 1/16 or 1/64 of the line data rate
- Selectable RX clock and RX data squelch
- Selectable timing modes/cleanup are field-configurable
- Internal phase detector and charge pump for cleanup phase-locked loop (PLL) (external VCXO required)
- Broadcom Serial Control (BSC) interface compatible with Philips® I^2C standard
- Optional SPI interface
- Core voltage, 1V
- Low power: 600 mW

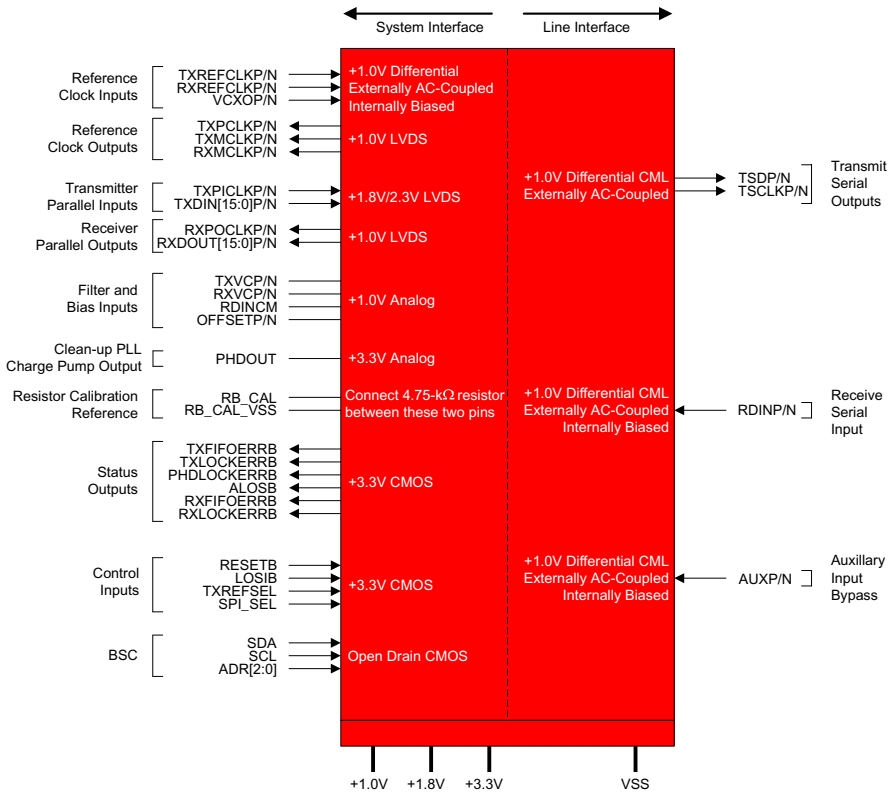
SUMMARY OF BENEFITS

- Enhanced capability for long haul transmission with the ability to enable RZ modulation on the transmitter
- Compliant with OIF, Telcordia®, ITU-T, XFI specification, and IEEE 802.3ae standards
- Input sensitivity 10 mV peak-to-peak
- Rates supported from 8.5 Gbps to 11.352 Gbps
- Fault isolation with loopbacks, pattern generator, and checker
- Reduces design cycle and time-to-market
- High-level of integration allows for higher port density solutions.
- Lowest power SFI-4 to 10G serial transceiver
- Standard CMOS 65 nm fabrication process

APPLICATIONS

- OC-192/STM-64/10-GbE/FEC transmission equipment
- SONET/SDH/10-GbE/10FC/FEC for RZ, NRZ or duo-binary optical modules
- ADD/DROP multiplexers
- Digital cross-connects
- ATM switch backbone
- SONET/SDH/10-GbE/10FC/FEC for NRZ, RZ, or duo-binary test equipment
- Terabit and edge routers

OVERVIEW



BCM8155 Interface Block Diagram

The BCM8155 is a fully integrated MSA-compatible multirate SONET/SDH/10-GbE/Fibre-Channel/FEC transceiver operating at 8.5 Gbps, 9.1 Gbps, 9.953 Gbps, 10.3125 Gbps, 10.519 Gbps, 10.664 Gbps, 10.709 Gbps, 11.095 Gbps, 11.318 Gbps, or 11.352 Gbps. It supports RZ, NRZ, and duo-binary modulation formats.

On-chip clock synthesis is performed by a high-frequency, low-jitter PLL, allowing the use of a low-frequency reference clock selectable to the line rate divided by 16 or 64. The 10G TX clock phase adjusts for clocked driver applications.

An on-chip phase detector and charge pump, plus external VCXO, implements a cleanup PLL. This can attenuate jitter on the CDR-recovered clock for loop timing applications, or provide a low-jitter reference from a noisy system clock. SONET timing modes can employ the new BCM8155 architecture, making timing mode and cleanup functions user-selectable in the field rather than during manufacturing. This simplifies engineering and manufacturing requirements.

The low-jitter LVDS interface guarantees compliance with the bit error rate requirements of the Telcordia (formerly Bellcore), ANSI, and ITU-T standards.

New features added to the BCM8155 include:

- Selectable RZ, NRZ and DB modulation
- Rates from 8.5 Gbps to 11.352 Gbps
- PRBS generator/checker for BIST
- Adaptive decision threshold adjustment
- Adjustable 10G TX clock phase
- 10G RX equalization for ISI compensation
- 10G TX preemphasis
- Differential duo-binary precoder
- BSC interface (compatible with Philips I^2C standard) or optional SPI interface

The BCM8155 is offered in two different packages:

1. 12 mm x 12 mm, 196-pin BGA (0.8 mm ball pitch)
2. 15 mm x 15 mm, 196-pin BGA (1 mm ball pitch)

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